Adequate Digital Baseband Processing

Trading off communication quality for power savings
by flexibly sacrificing processing accuracy

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Task

QoS-Adequate Baseband Radio Processing
(QoS-AB)

Task ID	:	2681.001
Thrust	:	AMS-CSD
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Students	:	Paul Detterer, PhD, expected graduation 2020
		Cumhur Erdin, PDEng, expected graduation September 2019

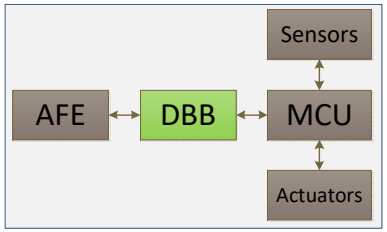
Adequate Computing

IoT needs ultra-low power, flexible communication

Trade
quality of communication for
power and energy

Architecture IoT Communication Node

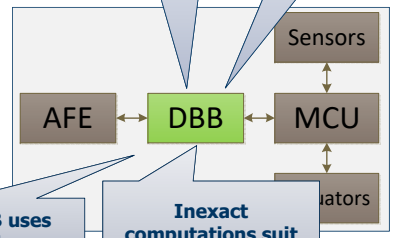
AFE – Analog Front End
DBB – Digital BaseBand
MCU – Micro Controller Unit



Architecture IoT Communication Node

Deals with noisy data from AFE and MCU

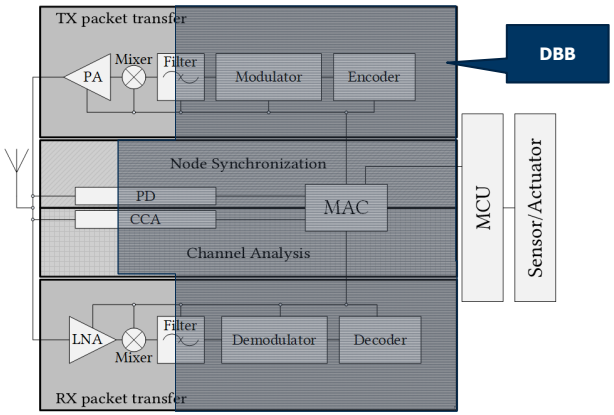
Power hungry in emerging IoT node designs



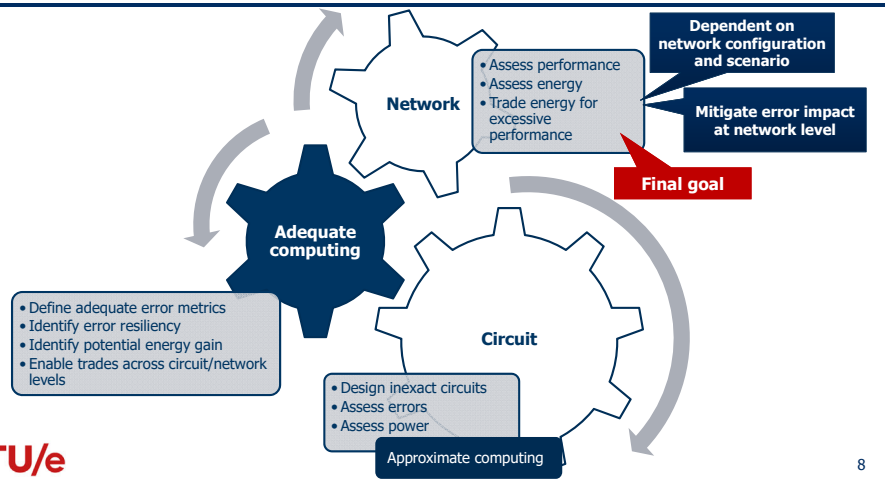
Conventional DBB uses exact computations

Inexact computations suit noisy data!

The DBB



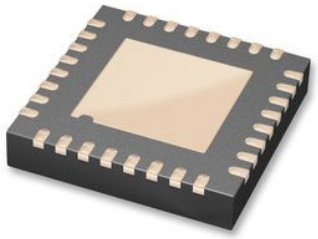
Adequate Computing



Circuit-level Power Reduction

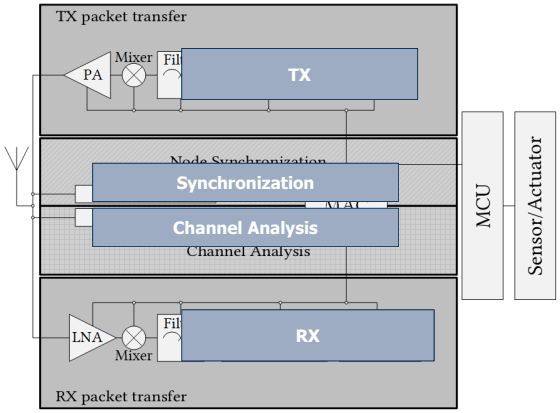
Methods:

- Reduce duty cycle ☑
- Clock gating ☑
- Power gating ☑
- Technology scaling ☑
- Efficient modulation ☑
- Approximate computing ?

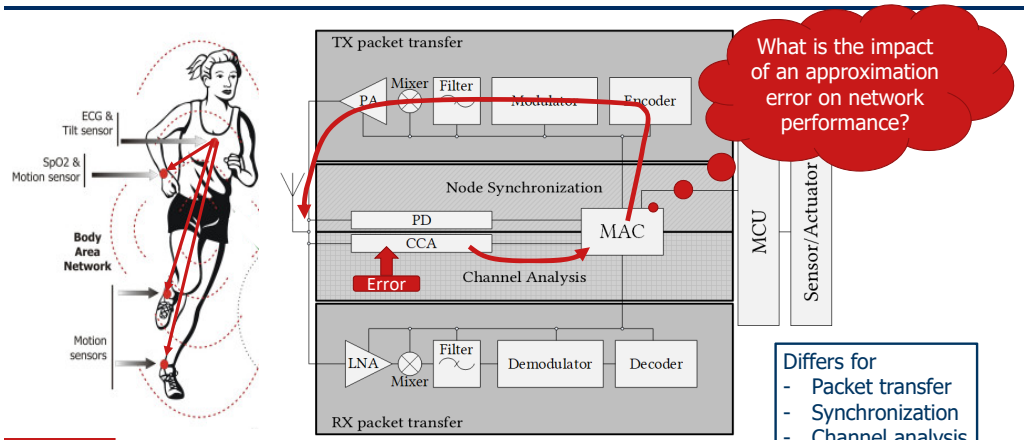


Opportunities

Four key operations in DBB



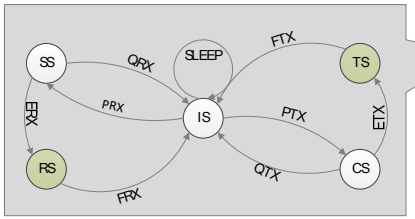
Impact of Approximation ?



Differs for
- Packet transfer
- Synchronization
- Channel analysis

Analysis: Network Simulation with Modified Nodes

Simulator: OMNet++



Modified network simulation

- State switching
- Sent packets
- Received packets
- Timing

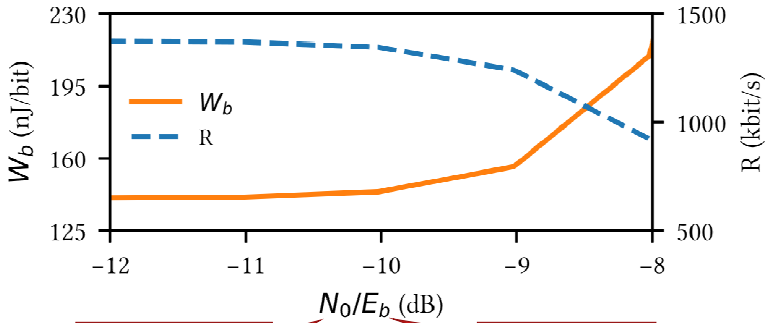
Postprocessing

R | L | W_b

Transceiver energy consumption per bit

Goodput | Latency

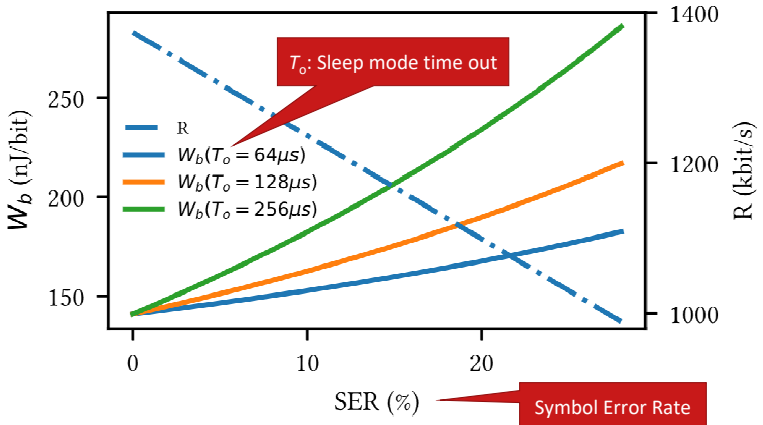
Impact of Approximate TX/RX



N_0 includes approximation noise

N_0: Noise density
E_b: Energy per bit

Impact of Approximate Synchronization

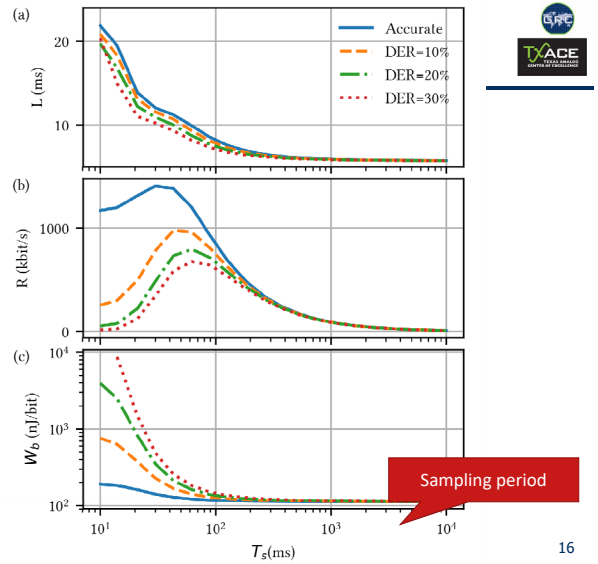


T_o: Sleep mode time out

Symbol Error Rate

CCA Approximation

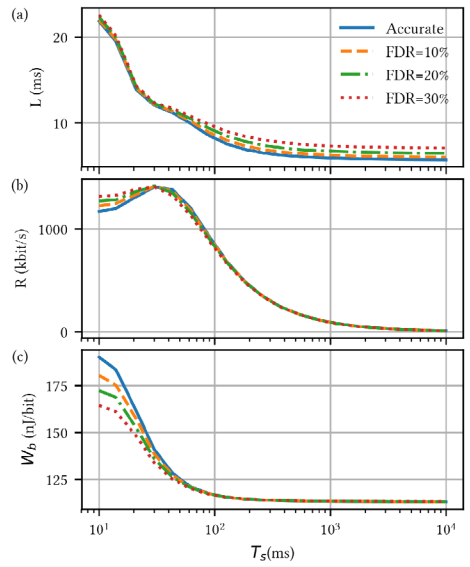
DER: Detection Error Rate



Sampling period

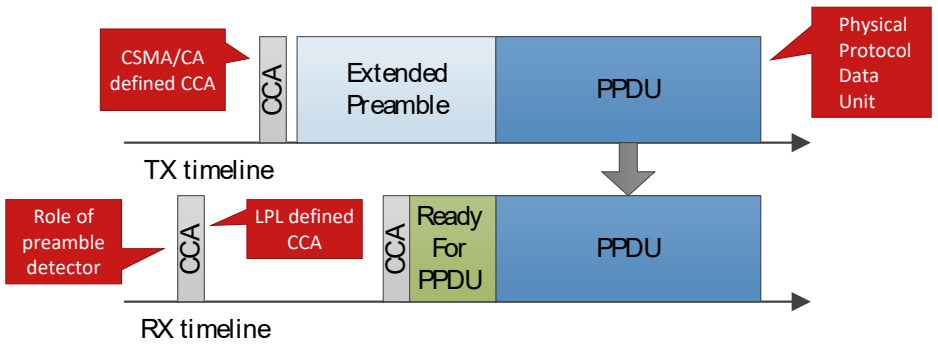
CCA Approximation

FDR: False Detection Rate

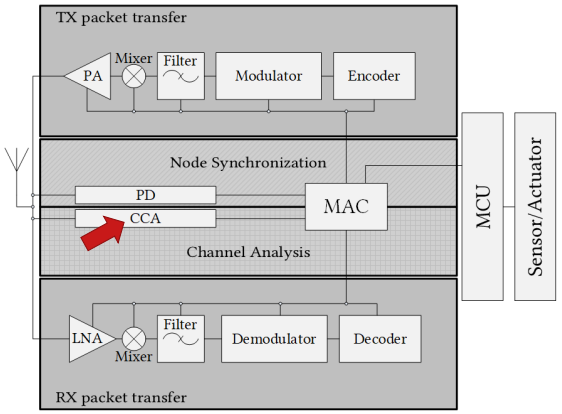


A Case Study

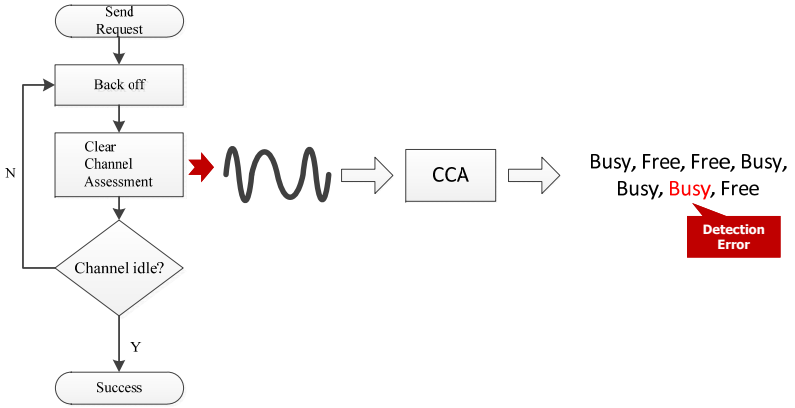
Low-Power Listening (LPL)



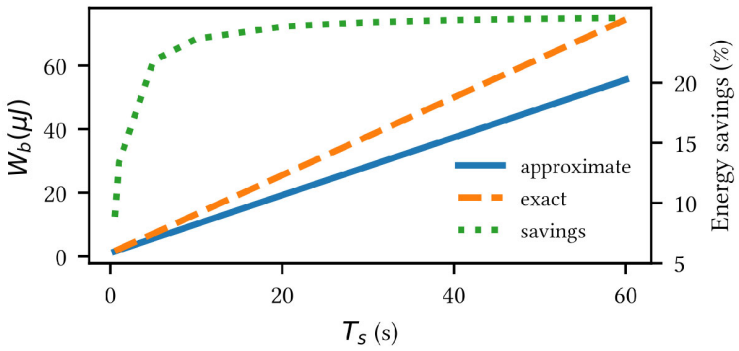
Approximating CCA in an LPL Scenario



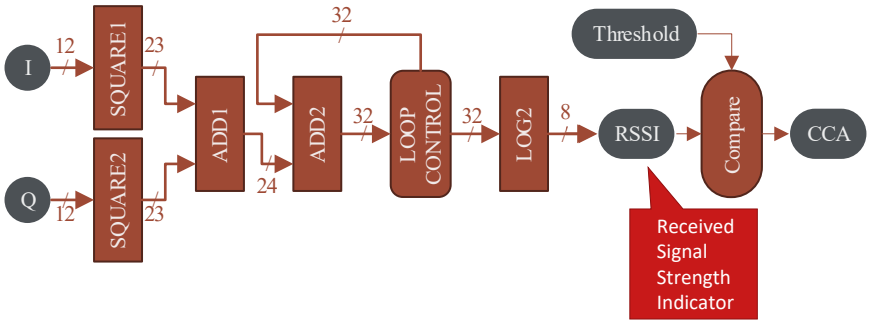
Approximating CCA



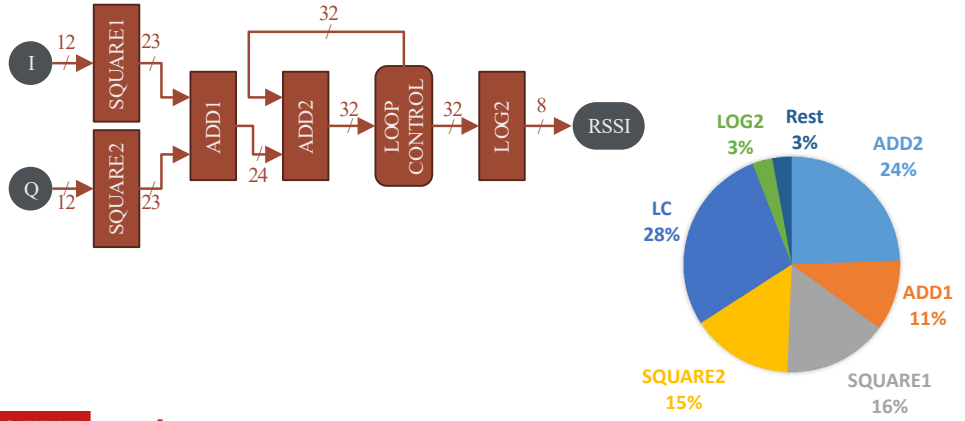
Approximating CCA in an LPL Scenario



RSSI-based CCA



RSSI Power Breakdown



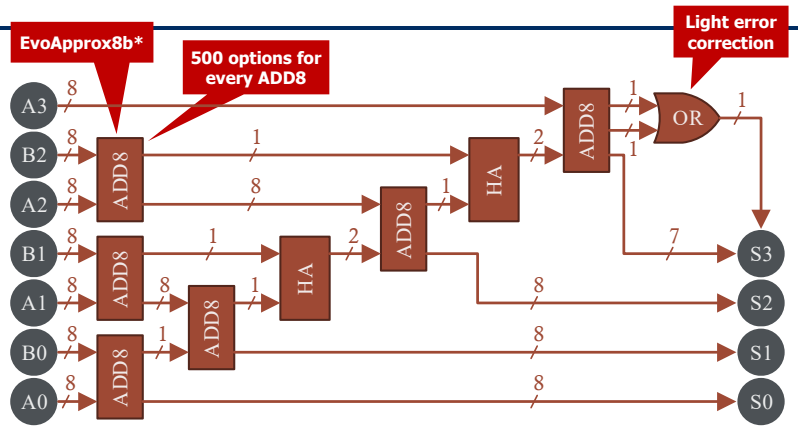
Approximation Approach

Combine different block-wise approximations

Analyze the combinations

Identify power-precision Pareto optimal combinations

ADD2 Approximation Template



* V. Mrazek, R. Hrbacek, Z. Vasicek, and L. Sekanina, "EvoApprox8b: Library of approximate adders and multipliers for circuit design and benchmarking of approximation methods," in *Proceedings of the IEEE/ACM Design, Automation & Test in Europe Conference & Exhibition*, 2017, pp. 258–261.

Pre-Selection

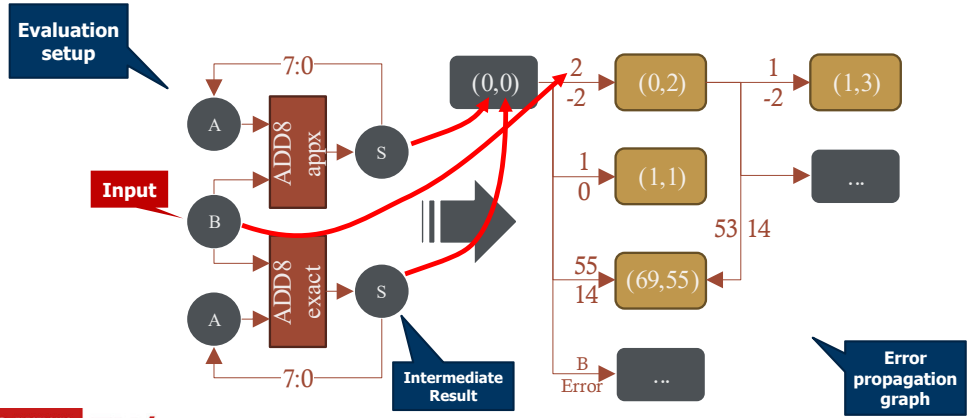
Power
- Only adders with sufficient power savings

0+0
- No adders with 0+0≠0 (bad for higher positions in the accumulator)

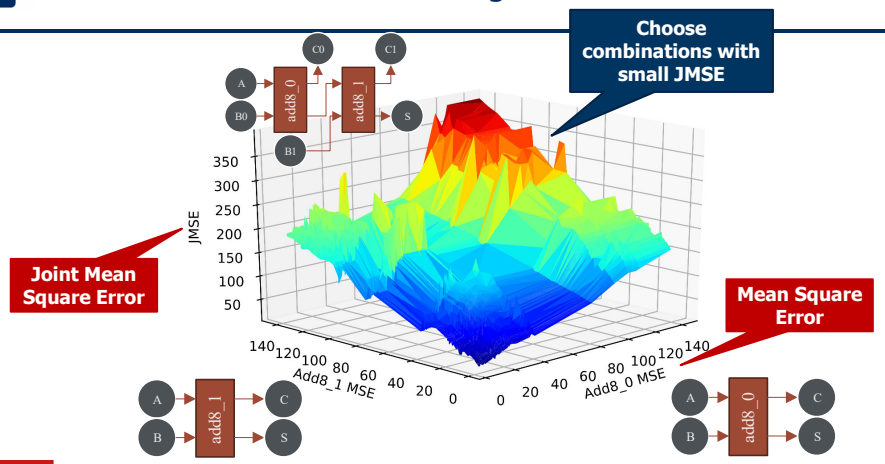
Self-accumulation
- No adders with self-accumulation effect

Pairing
- No adders with poor performance in cascade

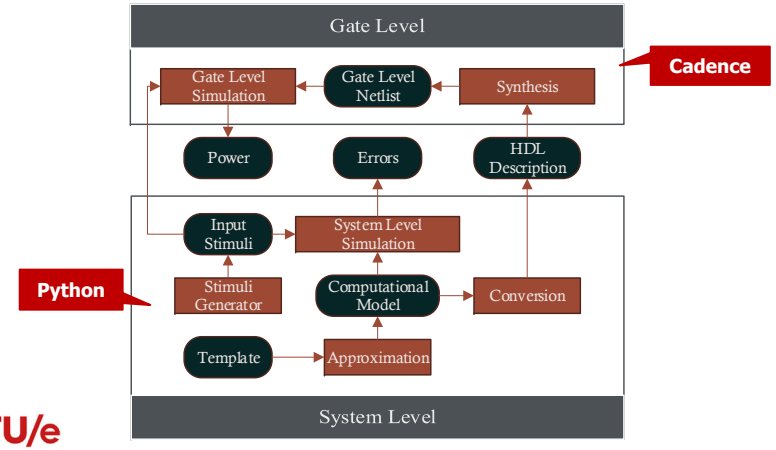
Self-Accumulation Analysis



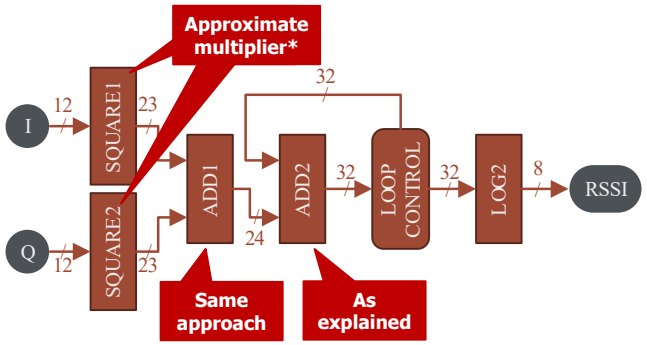
Pairing



Analysis Flow

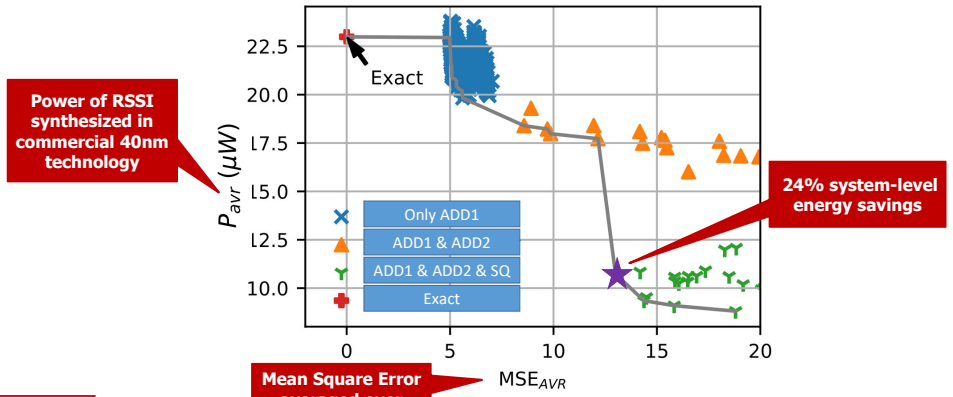


Approximation Overview

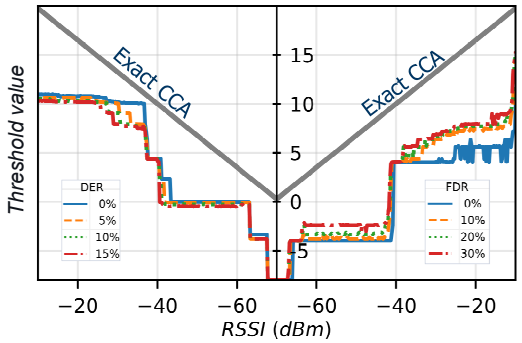


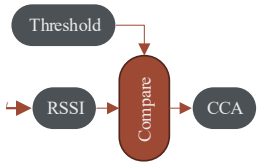
* K. Y. Kyaw et al., "Low-power high-speed multiplier for error-tolerant application," IEEE Int. Conf. Electron Devices and Solid-State Circuits, 2010.

Pareto Analysis



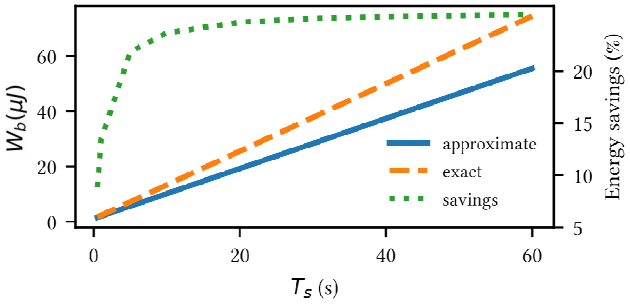
Configuring the CCA

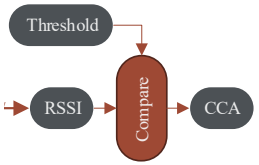




- Smart configuration of RSSI threshold
- Restricting the communication range

Approximating CCA in an LPL scenario

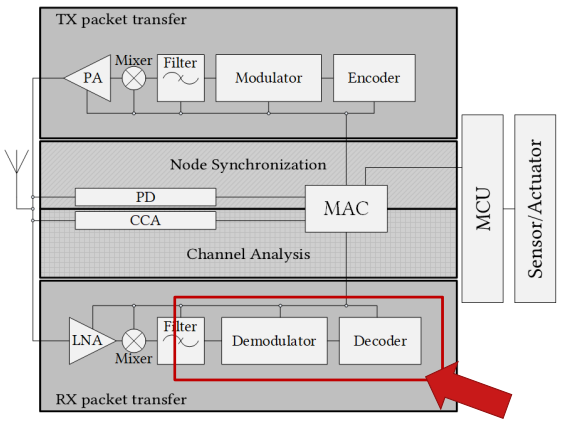




- Smart configuration of RSSI threshold
- Restricting the communication range

Other Opportunities

Approximating Packet Transfer

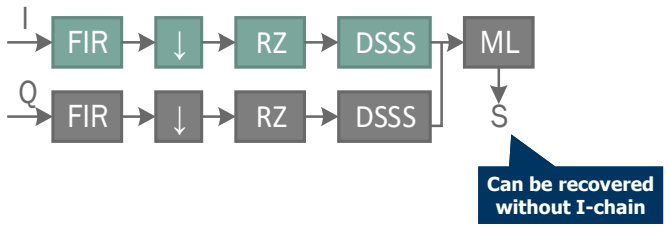


- Reduced bit width
- Bypassed filters
- Demodulator
- Decoder

Run-time adaptation would provide further opportunities!

Run-Time Adaptation

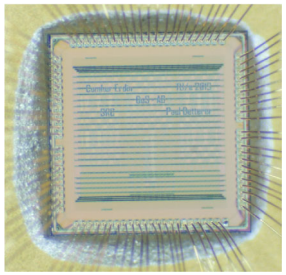
I-off RX Mode



Anticipated ~50% power savings for ~3 dB sensitivity loss

Evaluation SoC

Goals



- Trustworthy power reference
- Research vehicle

Chip Design Perspectives

- Energy efficient design
- Use combination of:
  - Approximation
  - Flexibility
  - Fine tuning

} Adaptive Design

How do we position ourselves?

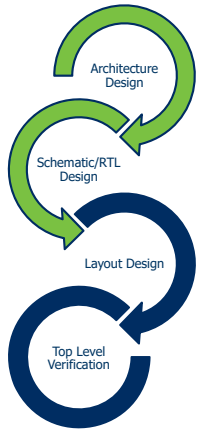
Adaptive Design }
- Auto adjustment according to channel conditions
- Decrease power when
  - ➢ possible
  - ➢ required

How do we do Energy Efficient Design?

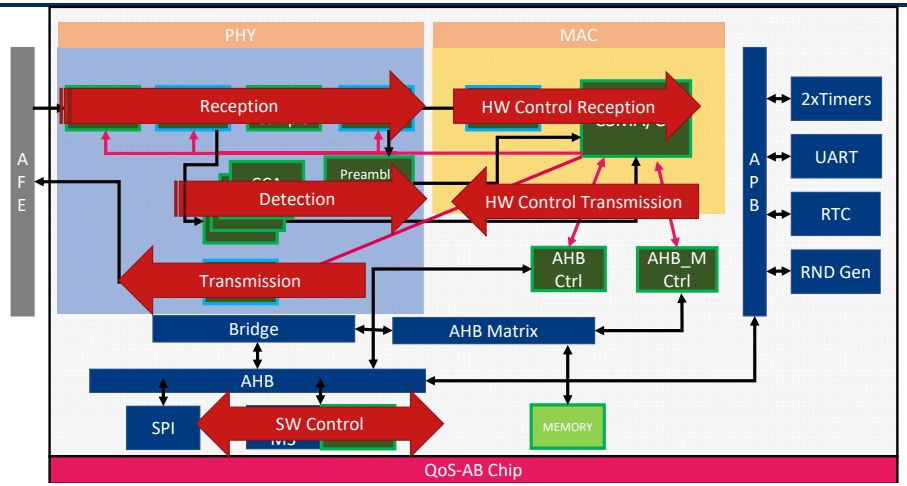
- Approximation – Reducing computational efforts
- Gating – Limiting usage of elements
- Configuration – Adjusting design parameters at run-time
- Hardware acceleration – Offloading MCU

Chip Tape-out Design Flow

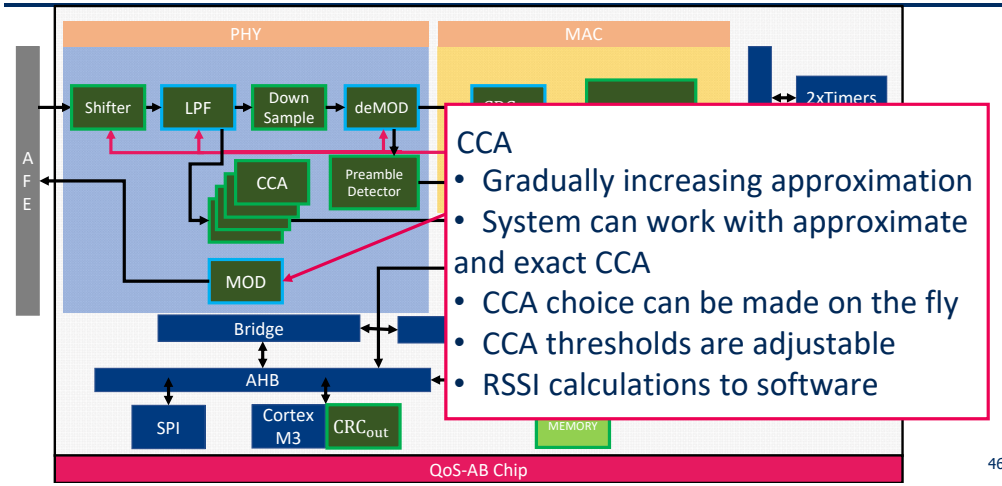
- Approximation – Reducing computational efforts
- Gating – Limiting usage of elements
- Configuration – Adjusting design parameters at run-time
- Hardware acceleration – Offloading MCU



Chip Architecture

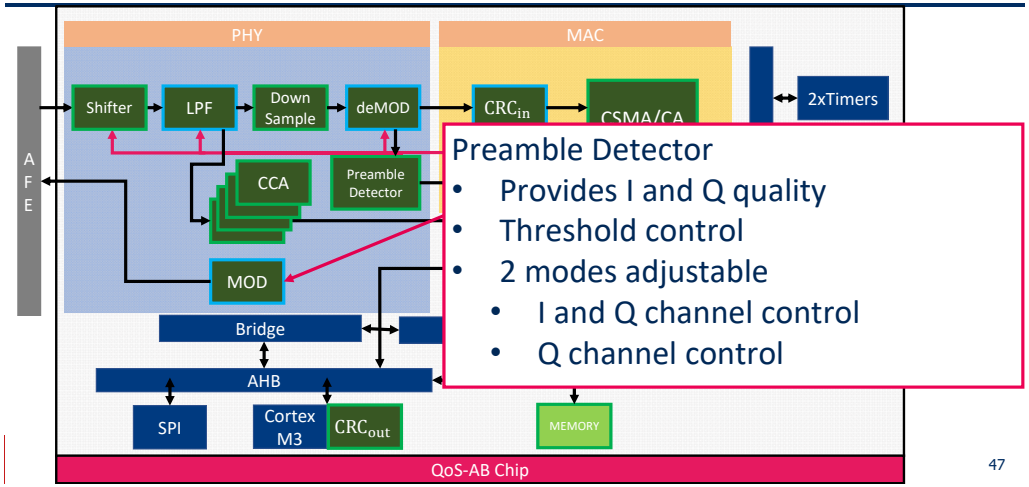


How are these methods used in CCA?



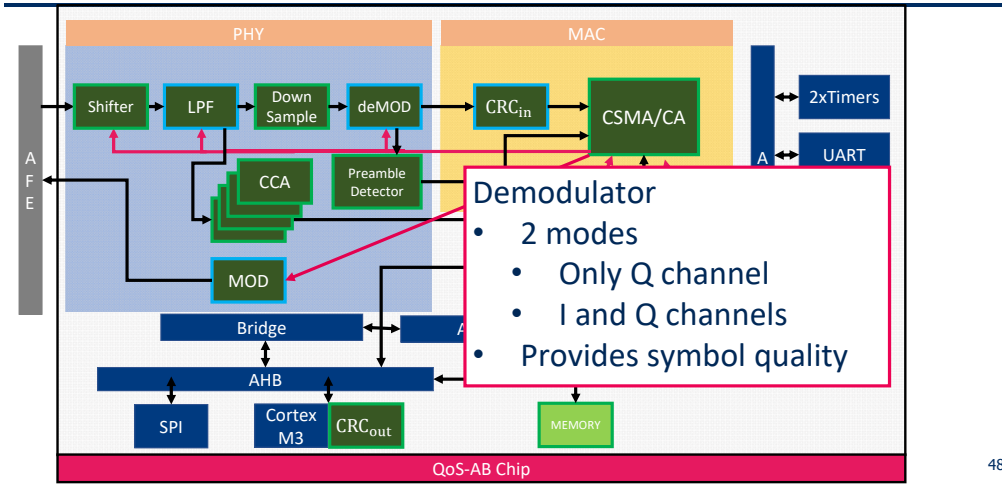
CCA
- Gradually increasing approximation
- System can work with approximate and exact CCA
- CCA choice can be made on the fly
- CCA thresholds are adjustable
- RSSI calculations to software

How are these methods used in Preamble Detector?



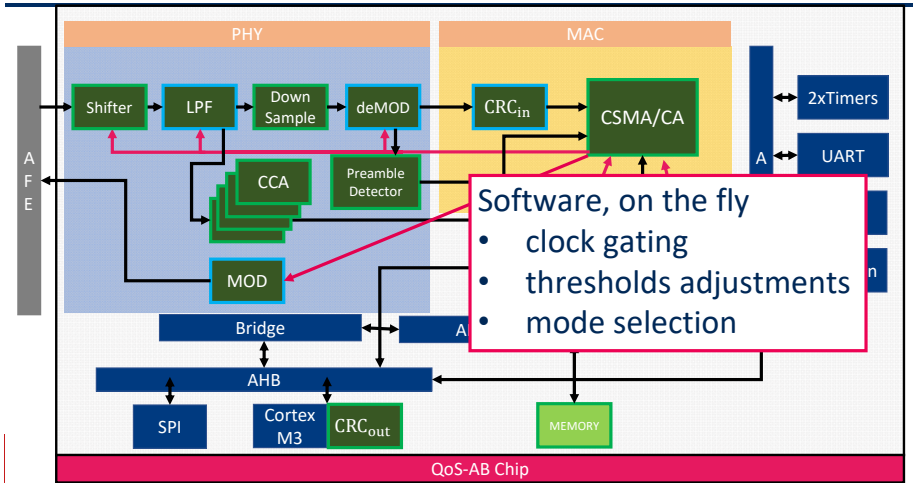
Preamble Detector
- Provides I and Q quality
- Threshold control
- 2 modes adjustable
  - I and Q channel control
  - Q channel control

How are these methods used in Demodulator?

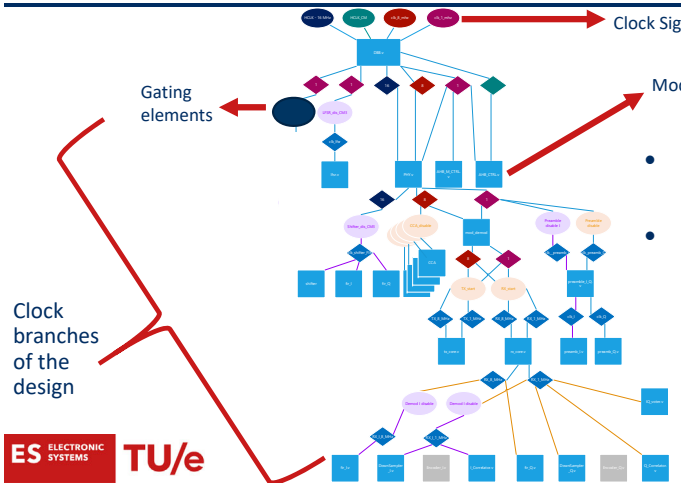


Demodulator
- 2 modes
  - Only Q channel
  - I and Q channels
- Provides symbol quality

How are these methods used in Software?

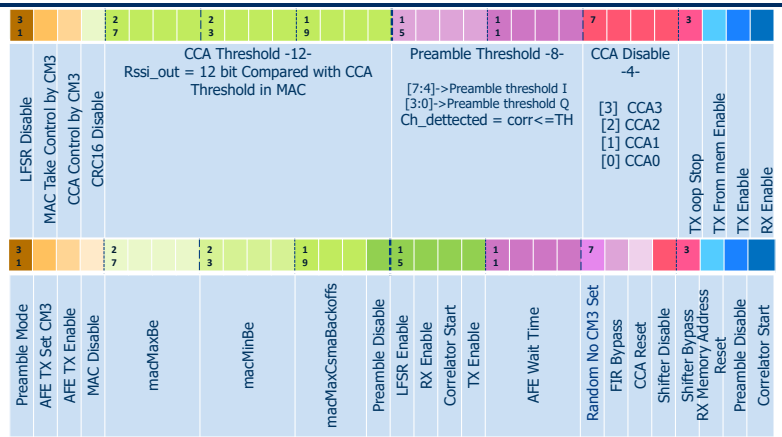


Smart Clock Gating

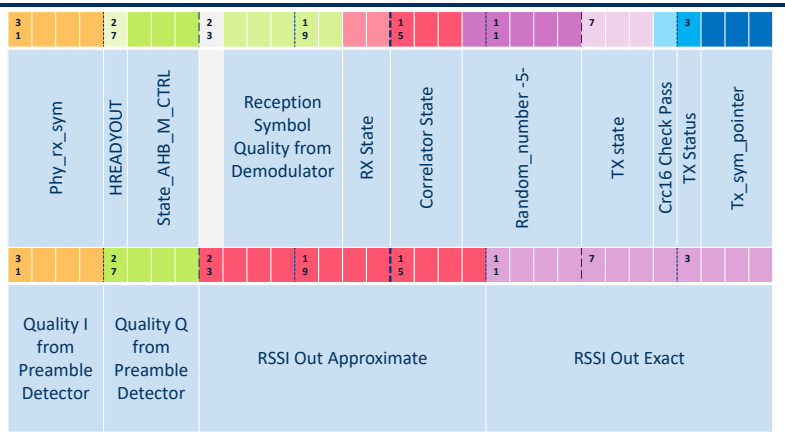


- Meaningful operating modes (e.g. I-off mode)
- Maximize power savings

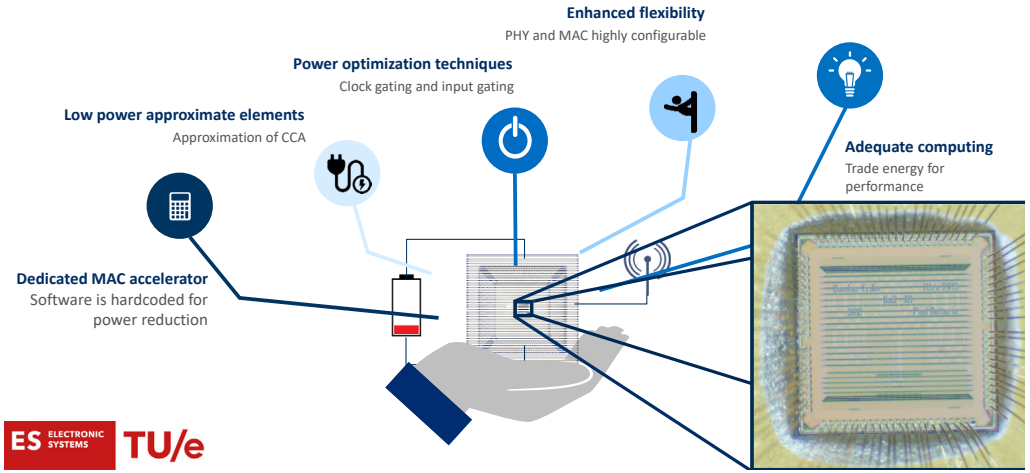
Configuration of PHY/MAC Accelerator



Information Transfer to the Software



Tape-out Conclusions



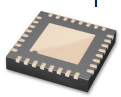
Conclusions

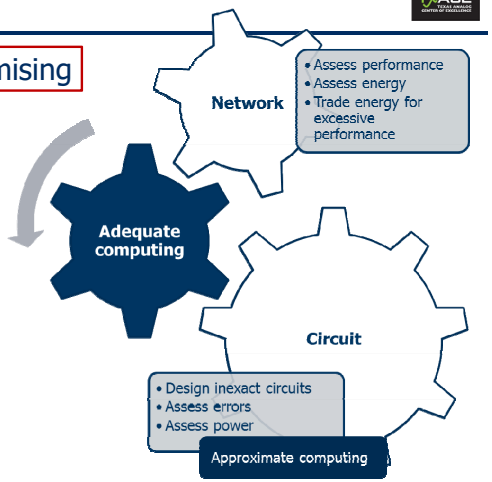
Conclusion

Adequate baseband processing is promising

Circuit-level power reduction:

- Reduce duty cycle ☑
- Clock gating ☑
- Power gating ☑
- Technology scaling ☑
- Efficient modulation ☑
- Approximate computing ☑





Questions ?

Adequate baseband processing is promising

Circuit-level power reduction:

- Reduce duty cycle ☑
- Clock gating ☑
- Power gating ☑
- Technology scaling ☑
- Efficient modulation ☑
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